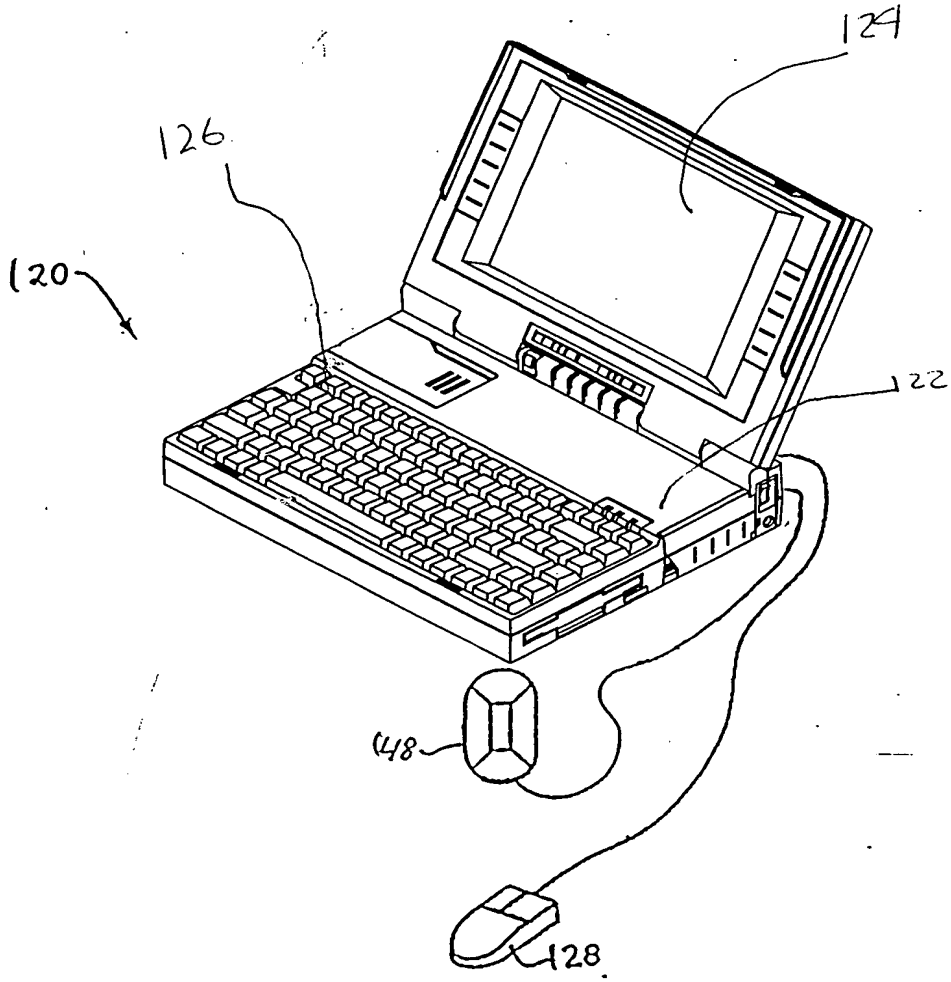

FIG 1

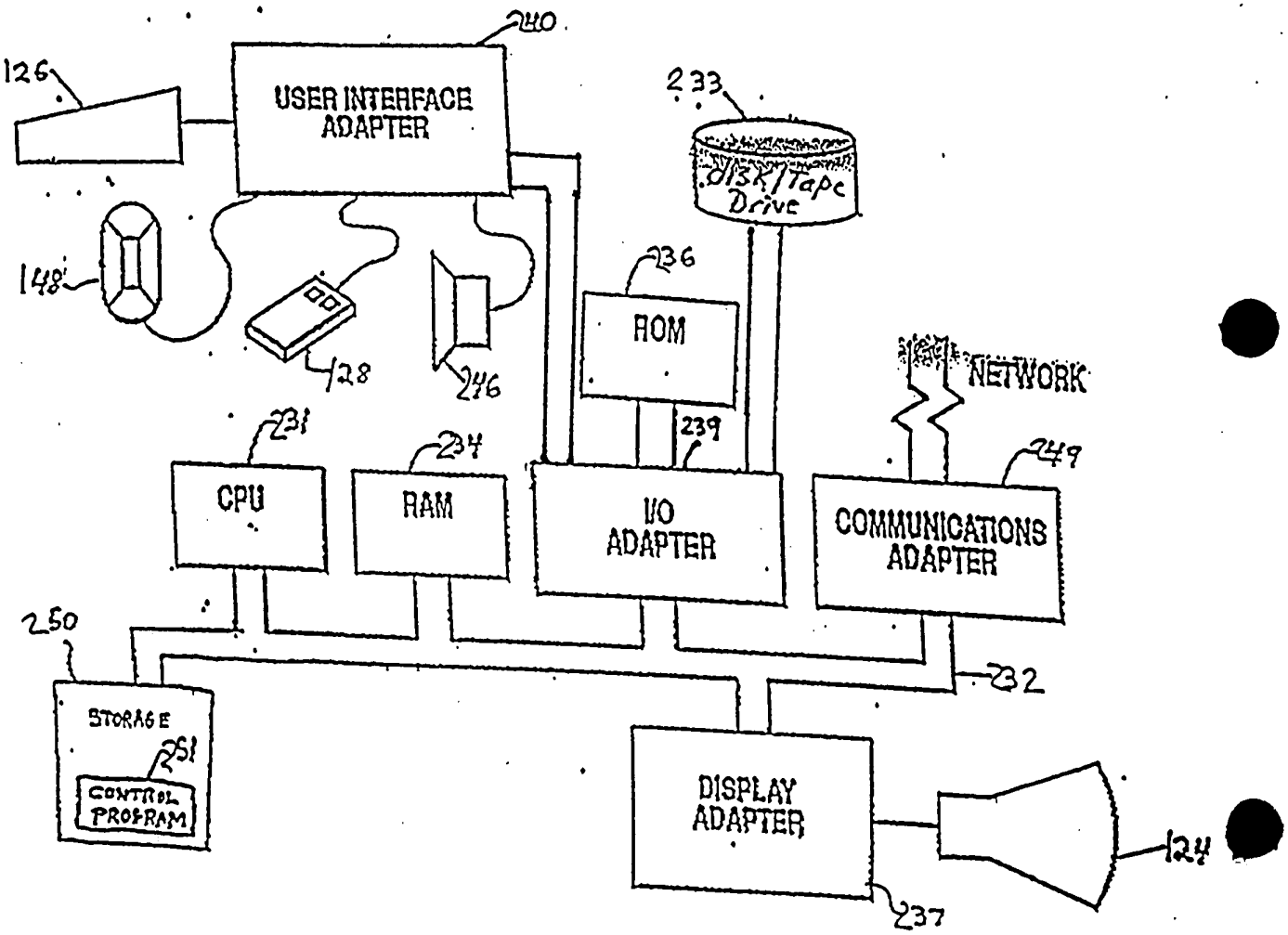
240
126
USER INTERFACE ADAPTER
233
DISK/Tape Drive
148
128
246
236
ROM
NETWORK
239
231
234
249
CPU
RAM
I/O ADAPTER
COMMUNICATIONS ADAPTER
250
232
STORAGE
251
CONTROL PROGRAM
DISPLAY ADAPTER
124
237
120

FIG. 2

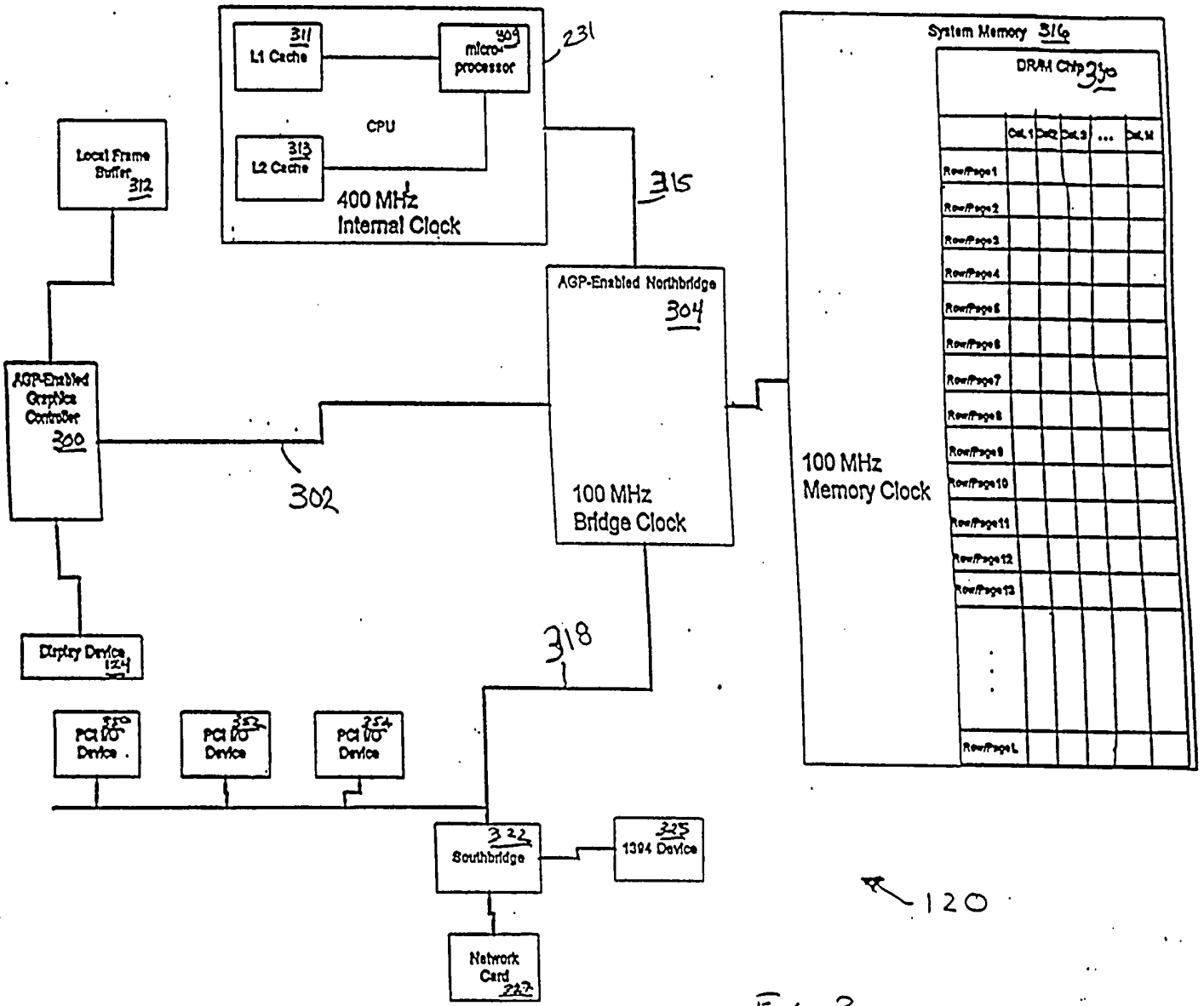
L1 Cache 311
micro-processor 309
231
CPU
L2 Cache 313
400 MHz Internal Clock
315
Local Frame Buffer 312
AGP-Enabled Northbridge 304
AGP-Enabled Graphics Controller 200
302
100 MHz Bridge Clock
System Memory 316
DRAM Chip 330
Col 1
Col 2
Col 3
...
Col M
Row/Page1
Row/Page2
Row/Page3
Row/Page4
Row/Page5
Row/Page6
Row/Page7
Row/Page8
Row/Page9
Row/Page10
Row/Page11
Row/Page12
Row/Page13
Row/PageL
100 MHz Memory Clock
318
Display Device 124
PCI I/O Device 350
PCI I/O Device 352
PCI I/O Device 354
Southbridge 322
1394 Device 325
Network Card 327
120

Fig. 3

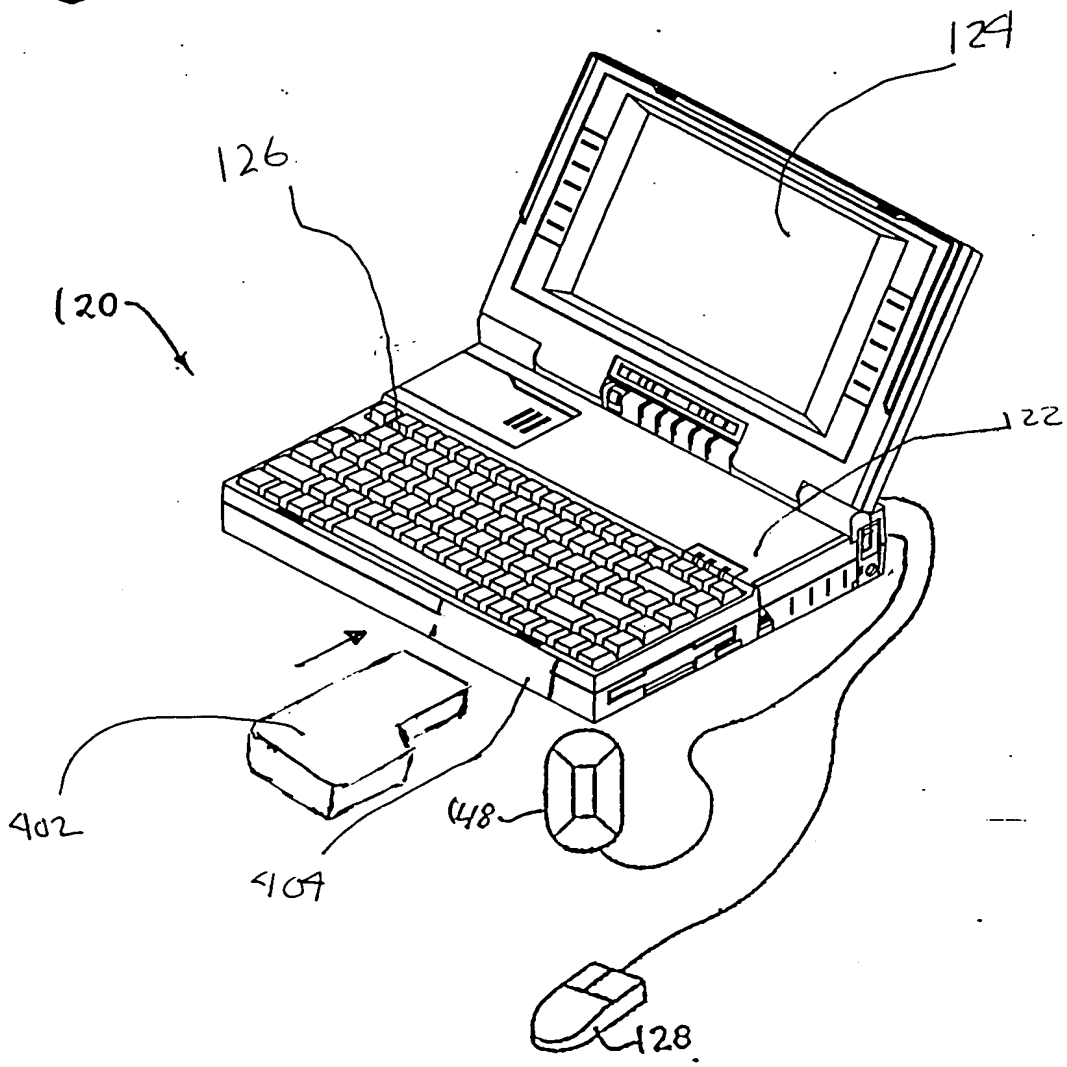

FIG 4

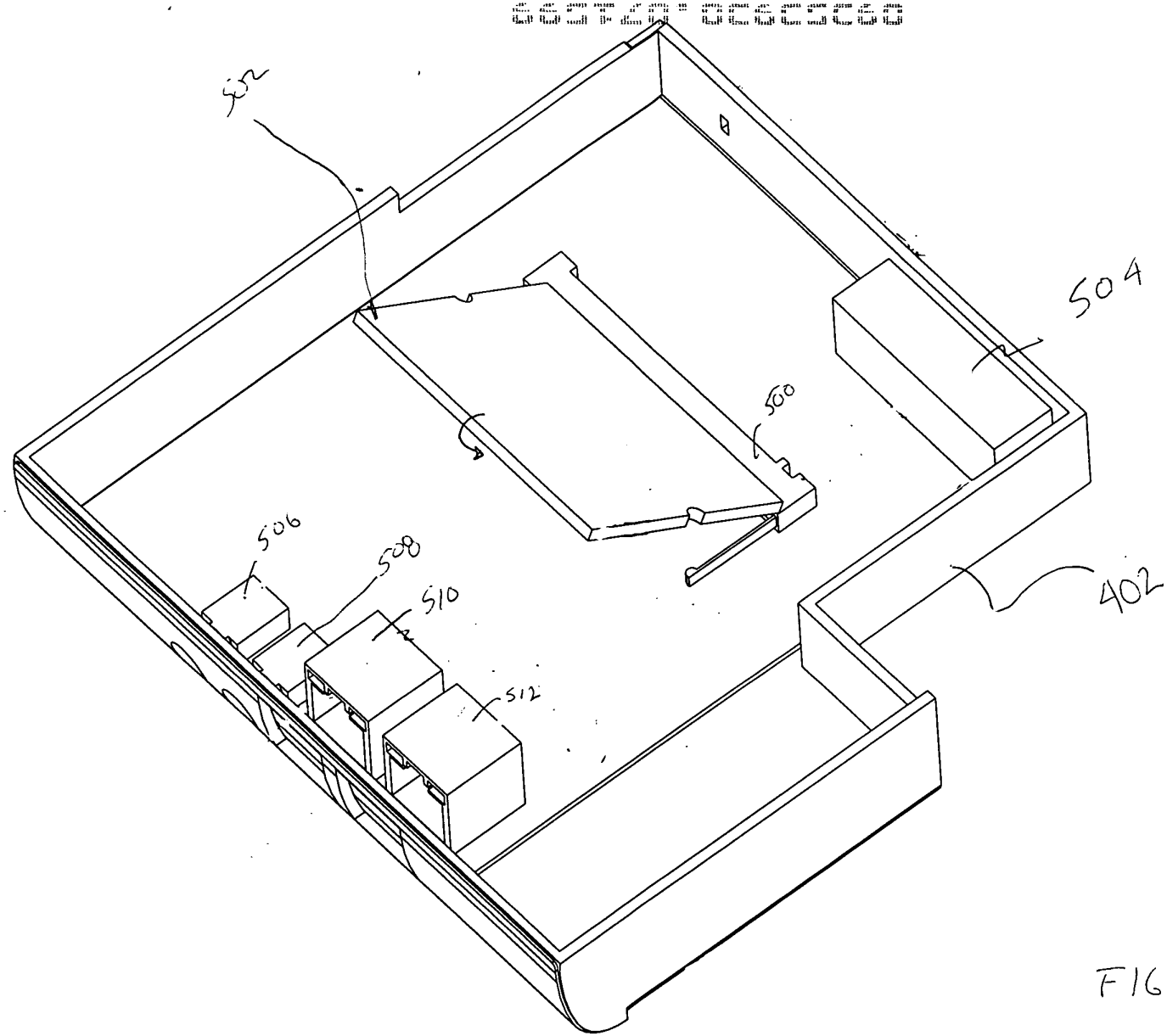

FIG. 5A

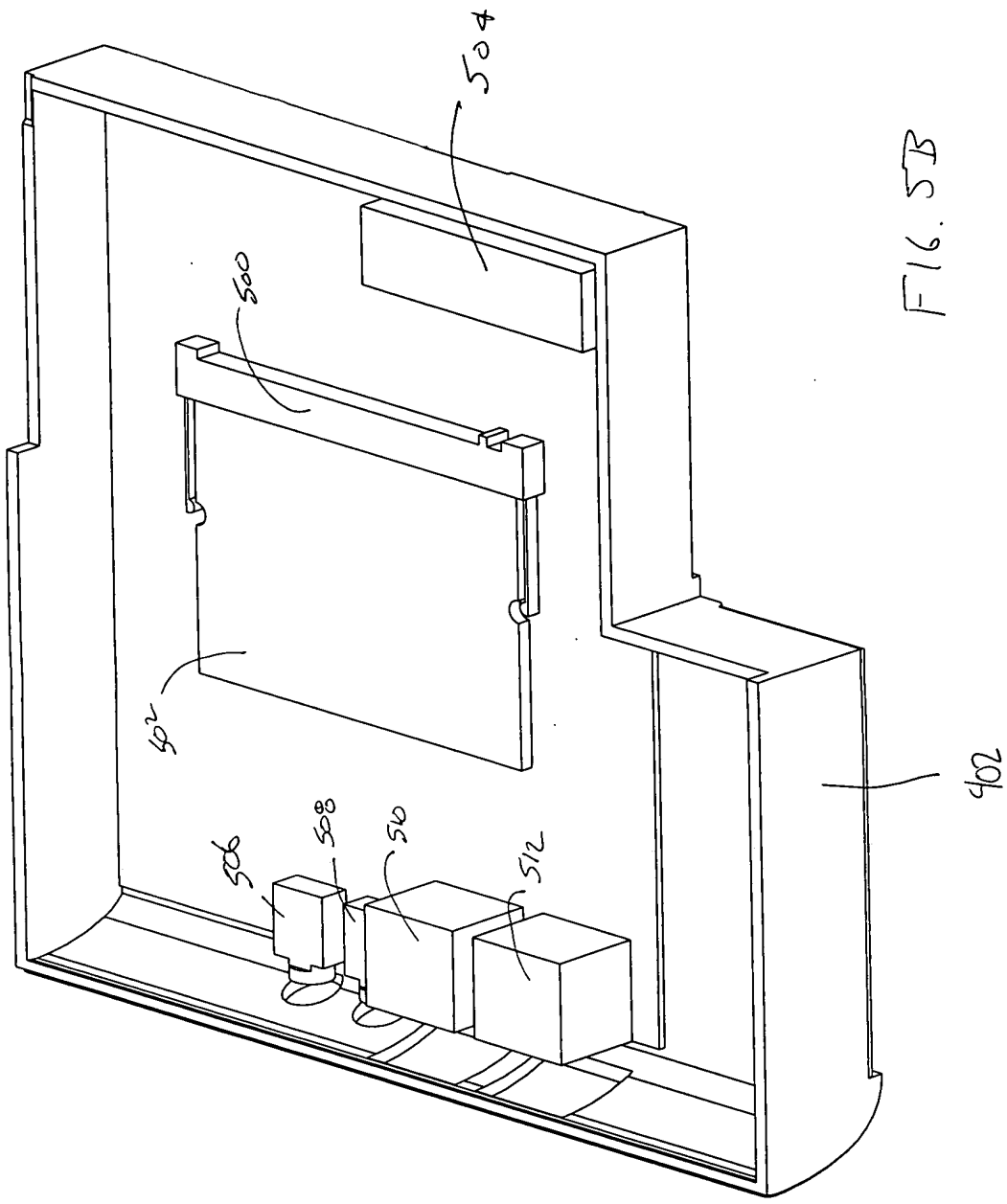

FIG. 5B

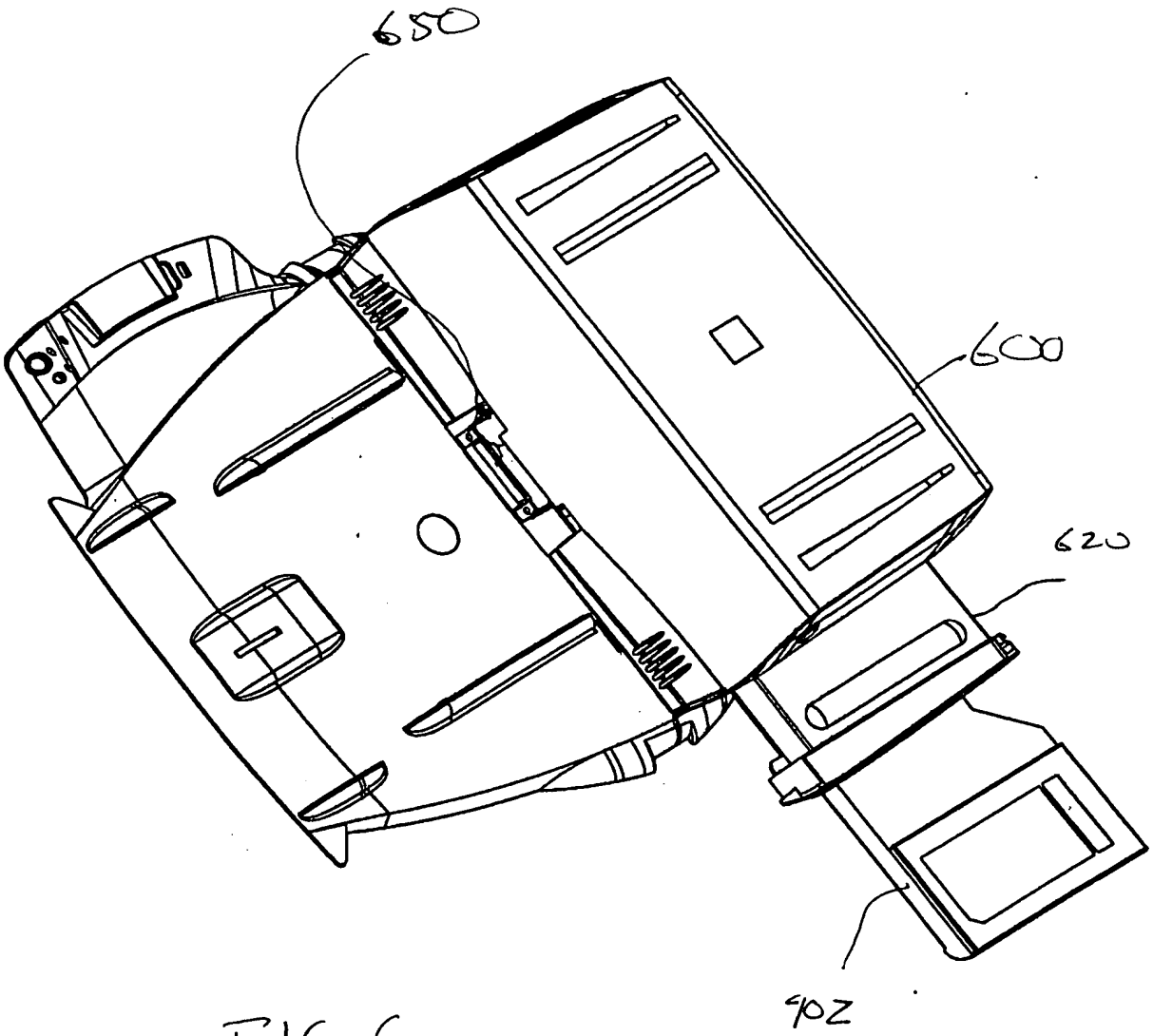

FIG. 6